PATENT ABSTRACTS OF JAPAN

(11)Publication number : 04-335431
(43)Date of publication of application : 24.11.1992

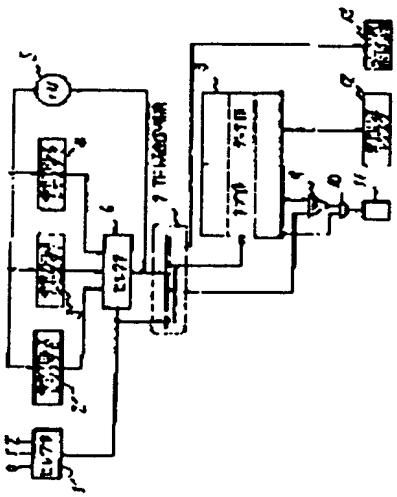
(51)Int.Cl. G06F 9/38
G06F 12/02
G06F 12/08
G06F 12/10

(21)Application number : 03-106252
(22)Date of filing : 13.05.1991

(71)Applicant : NEC CORP
(72)Inventor : SAKAI NORIAKI

(54) INFORMATION PROCESSOR

(57)Abstract:
PURPOSE: To eliminate the confliction between instruction prefetch addresses of different streams, and to efficiently use the high speed address converting mechanism of a direct map system by synthesizing an address by the selected stream number and a part determined in advance of the instruction prefetch address and setting it as a read/write address, and setting the part determined in advance as a comparison address.
CONSTITUTION: In the information processor provided with an instruction prefetch mechanism for prefetching a multi-stream instruction by using plural instruction buffers and a high speed address converting mechanism of a direct map system, the stream number given in advance to each instruction stream is selected by a selector 6, and an instruction prefetch address related to this instruction stream is selected. An address is synthesized by the selected stream number and a part determined in advance of the instruction prefetch address, its output is set as a read/write address, the part determined in advance is set as a comparison address and index and registration are executed.



LEGAL STATUS

[Date of request for examination]

[Date of sending the examiner's decision of rejection]

[Kind of final disposal of application other than the examiner's decision of rejection or application converted registration]

[Date of final disposal for application]

[Patent number]

[Date of registration]

[Number of appeal against examiner's decision

of rejection]
[Date of requesting appeal against examiner's decision of rejection]
[Date of extinction of right]